UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/246,582	05/19/94	SAWADA S	3941597

ZARABIAN, EXAMINER

25M1/0608

LOWE, PRICE, LEBLANC, BECKER & SHUR
99 CANAL CENTER PLAZA
SUITE 300
ALEXANDRIA, VA 22314

ART UNIT	PAPER NUMBER
2511	9

DATE MAILED: 06/08/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☒ Responsive to communication filed on 3-31-95 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 1-36 are pending in the application.
   Of the above, claims 6-8 and 34-36 are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-5, 9, 10, 12-14 and 31-33 are rejected.
5. ☒ Claims 11 and 15-30 are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☒ The proposed additional or substitute sheet(s) of drawings, filed on 5-31-95 has (have) been ☒ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

Claims 2, 4, 5 and 9 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, lines 11 and 19, "data output terminals", it is not clear if this is the same terminal as in line 5. In line 16, "readmeans" it is not clear if this is the same "means" as in line 6.

In claim 4, line 8, "arrays" has no antecedent basis, in line 14, "memory cell", it is not clear if this is the same "cell" as in line 5.

In claim 5, line 15, "memory cell array", it is not clear if this is the same cell as in line 5, in line 18, "data output terminals" it is not clear if this is the same data output terminals as in line 10, in line 23, "memory cells" has no antecedent basis.

In claim 9, line 7, "memory cell array" it is not clear if this is the same "array" as in line 6.

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 1-3, 12-14 and 31-33 are rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Kawai.

Adams in figure 1 discloses a memory device responsive to a clock signal comprising, a memory cell array having plurality of cells (14), selection means (16) for selecting the memory cells, read means for reading the data and compressing means (32) responsive to test made for compressing the data indicating the defective memory and outputting data to output terminal (col. 3, lines 22-27). Adams further shows that failed address register (34) operate in synchronization with a clock signal (CL) but Adams does not disclose use of plurality of elements, output buffers and read registers and the structure of the data compressor.

The use of output buffers and read registers is well known in the art. Kawai discloses a flip flop circuit where F/F, 201-208 function as a compressor for compressing a plurality of data read from memory array (or arrays) in synchronization with clock signal pulses and providing an output to a terminal (104) (see col. 2, lines 48-49 and col. 6, lines 61-65). Therefore it would have been obvious to use plurality of arrays, output buffer and register and a synchronous compressor; such as compressor of

Kawai, as the compressor in the system of Adams for compressing the synchronous read data from the memory array of Adams.

Claims 4 and 5 are rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Kawai in view of Getzlaff in view of An.

Adams in view of Kawai as applied in prior rejection discloses every claimed subject matter except the use of a precharger and a subcompressor.

Getzlaff shows a compressor performing logical operations and having smaller subcompressor (col. 2, lines 42-45). An as disclosed in prior rejections teaches the use of a precharger. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a precharger, such as An's; to charge the bitlines and to use a two stage compressor performing logical operative, such as Getzlaff's, in place of data compressor (32) of Adams in order to compress the data.

Claim 10 is rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Getzlaff.

Adams as applied in prior rejection discloses a read means (16, 18 ...) for reading data of memory cells into a data compressor (32), but Adam does not teach the details of the compressor. Getzlaff as applied in prior rejection in figure 5A teaches the use of a compressor having a first wired circuit having plurality of n-channel FET each having a gate receiving a

data read signals (C1, D1) and being connected in parallel to a first signal (GND), a second wired circuit having p-channel FET, receiving read signals (Bo, B1) and being coupled in parallel to a second signal (VDD). The outputs of the wired circuits are connected to logic means. Therefore it would have been obvious to one of ordinary skill in the art to use the compressor of Getzlaff in place of data compressor (32) of Adams in order to compressor the data read from the memory cell array.

Claim 9 is rejected under 35 U.S.C. § 103 as being unpatentable over Ueoka in view of Kawai.

Ueoka in figures 1 and 2 discloses a memory device pulsed clock signal (fig. 4) comprising a plurality of banks (11) including memory arrays, activating means for simultaneously activating plurality of banks in a test mode (Abst) and activating a block response to block address during a normal operation, but Ueoka is not synchronous. Kawai as applied in prior rejection discloses reading an array in synchronous with a pulsed clock. Therefore it would have been obvious to one of ordinary skill to read data in a block of Ueoka in synchronous with a clock during normal made and all the blocks during a test mode.

Claims 11 and 15-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art does not disclose a generation means responsive to prechargenable signal (as in claim 16) and the relationship between prescribed number of data registers and predetermined number of memory cells (as in claims 19 and 29).

Any inquiry concerning this communication should be directed to A. Zarabian at telephone number (703) 308-4905.

Zarabian/tj

June 5, 1995

A. Zarabian
AU. 2511